IN THE CLAIMS:

1. (Currently Amended) A method for preventing contention on a data bus connecting a central processing unit and a peripheral device when the central processing unit calls for a read operation followed by a write operation, comprising:

connecting a transceiver with bus hold circuitry and an output enable input in the data bus between the central processing unit and the peripheral,

generating a control signal which ends at a preselected time before the end of the read operation, and,

providing the control signal to an input of the peripheral and to the output enable input of the transceiver.

2. (Original) The method of Claim 1 further including;

connecting a buffer having an output enable input between an address output of said central processing unit and an address input of said peripheral device, and

providing a chip select signal to the output enable input of said buffer.

3. (Original) The method of Claim 1 wherein said preselected time is equal to or greater than the maximum time to enable high impedance state of said transceiver.

4. (Original) The method of Claim 1 wherein said preselected time is greater than fifty nanoseconds.

5. (Currently Amended) Apparatus for preventing contention on a data bus connecting a central processing unit and a peripheral device when the central processing unit calls for a read operation followed by a write operation, comprising:

a transceiver with bus hold circuitry and an output enable input connected between the data bus input/output connections of the central processing unit and the peripheral, and

control logic having an input for receiving a CPU chip select signal and an output for providing a peripheral control signal which ends at a preselected time before the end of the read operation,

said control logic output connected to a control input of the peripheral and to the output enable input of the transceiver.

6. (Currently Amended) The apparatus of Claim 5, further including;

a buffer connected between an address output of said central processing unit and an address input of said peripheral device, said buffer having an output enable input connected to ~~a~~ the chip select signal.

7. (Original) The apparatus of Claim 5 wherein said preselected time is equal to or greater than the maximum time to enable high impedance state of said transceiver.

8. (Original) The apparatus of Claim 5 wherein said preselected time is greater than fifty nanoseconds.

9. (Currently Amended) A method for controlling the reading of data by a processing unit from a peripheral device over a bidirectional data bus during a read operation, said peripheral device having a maximum time to enable high impedance state, comprising;

connecting a transceiver with bus hold circuitry and an output enable input in the data bus between the central processing unit and the peripheral,

generating a peripheral control signal which ends at a time equal to or greater than said maximum time to enable high impedance state before the end of the CPU read command, and,

providing the peripheral control signal to an input of the peripheral and to the output enable input of the transceiver.

10. (Original) The method of Claim 9, wherein said read operation occurs during eight clock cycles and said peripheral control signal ends one and one-half clock cycles before the end of the read operation.

11. (Original) Apparatus for controlling the reading of data by a processing unit from a peripheral device over a bidirectional data bus during a CPU read operation, said peripheral device having a control input and a maximum time to enable high impedance state, comprising;

a transceiver with bus hold circuitry connected between the data bus input/output connections of the central processing unit and the peripheral, said transceiver having an output enable input,

control logic having an input for receiving a CPU data strobe signal and an output for providing a peripheral control signal which ends at a time equal to or greater than said maximum time to enable high impedance state before the end of the read operation, and,

said control logic output connected to a control input of the peripheral and to the output enable input of the transceiver.

12. (Original) The apparatus of Claim 11 wherein said read operation occurs during eight clock cycles and said peripheral control signal ends one and one-half clock cycles before the end of the read operation.